What is claimed is:

1. A method for use in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly having a surface; and

forming a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

2. The method of claim 1, wherein x is in the range of about 1 to about 3.

3. The method of claim 2, wherein x is about 2.

4. The method of claim 1, wherein forming the barrier layer includes depositing $RuSi_x$ by chemical vapor deposition.

5. The method of claim 1, wherein forming the barrier layer includes:

forming a layer of ruthenium relative to a silicon containing region; and

performing an anneal to form $RuSi_x$ from the layer of ruthenium and the silicon containing region.

6. The method of claim 5, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by chemical vapor deposition.

7. The method of claim 1, wherein the method further includes forming at least one additional conductive material over the diffusion barrier layer, the at least one additional conductive material selected from a group of a metal and a conductive metal oxide.

8. The method of claim 5, wherein performing the anneal to form $RuSi_x$ includes performing an anneal at a temperature in the range of about 400° C to about 1000° C for about 0.5 minutes to about 60 minutes in an inert gas atmosphere.

9. The method of claim 8, wherein performing the anneal to form $RuSi_x$ includes annealing the layer of ruthenium and the silicon containing layer at a temperature of about 500° C for about 5 minutes in a nitrogen atmosphere.

10. The method of claim 5, wherein silicon containing region includes the at least a portion of the surface.

11. A method for use in the formation of a capacitor, the method comprising:

forming a first electrode on a portion of a substrate assembly;

forming a high dielectric material over at least a portion of the first electrode; and

forming a second electrode over the high dielectric material, wherein at least one of the first and second electrodes comprises a barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

12. The method of claim 11, wherein x is in the range of about 1 to about 3.

13. The method of claim 12, wherein x is about 2.0.

14. The method of claim 11, wherein the barrier layer is formed by chemical vapor deposition.

15. A method for use in the formation of a capacitor, the method comprising:

providing a silicon containing region of a substrate assembly;

forming a first electrode on at least a portion of the silicon containing region of the substrate assembly, the first electrode comprising a barrier layer of $RuSi_x$, where x is in the range of about 0.01 to about 10;

providing a high dielectric material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric material.

16. The method of claim 15, wherein x is in the range of about 1 to about 3.

17. The method of claim 15, wherein forming the barrier layer includes:

forming a layer of ruthenium on the at least a portion of the silicon containing region; and

annealing the layer of ruthenium formed on the at least a portion of the silicon containing region resulting in the $RuSi_x$ barrier layer.

18. The method of claim 17, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by chemical vapor deposition, the layer of ruthenium having a thickness of about 10Å to about 300Å.

19. The method of claim 18, wherein the layer of ruthenium has a thickness of about 50Å to about 200Å.

20. The method of claim 19, wherein the layer of ruthenium has a thickness of about 100Å.

21. The method of claim 18, wherein annealing the layer of ruthenium formed on the at least a portion of the silicon containing region includes annealing at a temperature in the range of about 400° C to about 1000° C for about 0.5 minutes to about 60 minutes in an inert gas atmosphere.

22. The method of claim 15, wherein the $RuSi_x$ barrier layer is formed by chemical vapor deposition using a ruthenium precursor and a silicon precursor.

23. A method for use in the formation of a capacitor, the method comprising:

providing a silicon containing region of a substrate assembly;

forming a first electrode on at least a portion of the silicon containing region of the substrate assembly, the forming of the first electrode comprising:

forming a barrier layer of $RuSi_x$, where x is in the range of about 0.01 to about 10, and

forming one or more conductive layers relative to the $RuSi_x$ barrier layer, the one or more conductive layers formed of at least one of a metal or a conductive metal oxide;

providing a high dielectric material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric material.

24. The method of claim 23, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

25. The method of claim 23, wherein forming the barrier layer includes:

forming a layer of ruthenium on the at least a portion of the silicon containing region; and

annealing the layer of ruthenium formed on the at least a portion of the silicon containing region resulting in the $RuSi_x$ barrier layer.

26. The method of claim 23, wherein the $RuSi_x$ barrier layer is formed by chemical vapor deposition using a ruthenium precursor and a silicon precursor.

27. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. The structure of claim 23, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a diffusion barrier layer formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. The structure of claim 32, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$, where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.

38. The structure of claim 36, further comprising a conductive contact material formed relative to the diffusion barrier layer.